AMENDMENTS TO THE CLAIMS

1. (Previously Presented) A method for time multiplexing signals comprising:

performing an initial routing of the set of nets;

identifying nets comprising signal sources having associated programmable

interconnects in substantially the same area;

merging a set of nets carrying the signals into a shared interconnect portion;
altering a netlist based on the merging; and

placing a design represented by the altered netlist.

2. (Previously Presented) A method of time multiplexing signals on interconnect in a

programmable logic device, the method comprising:

merging the nets into a shared interconnect portion;

altering the design based on the merging;

placing the altered design; and

routing the altered design; and

wherein the altered design comprises a plurality of source configurable logic

blocks and a plurality of destination configurable logic blocks.

3. (Previously Presented) An integrated circuit comprising:

a set of configurable logic blocks comprising multiple signal sources and at

least one destination;

a time multiplexing signal generator controlling which of the multiple signal sources

provides its signal to a corresponding signal destination; and

a programmable interconnect coupled between an output of the time multiplexing

signal generator and a destination configurable logic block.

4. (Previously Presented) The integrated circuit of Claim 3, wherein the multiple

signal sources are located in one configurable logic block.

5. (Previously Presented) The integrated circuit of Claim 3, wherein the multiple signal sources generate critical signals.

6. (Previously Presented) The integrated circuit of Claim 3, wherein the time multiplexing signal generator includes a counter.

7. (Previously Presented) The method of Claim 1, further comprising a step of analyzing nets for high latency signals.

8. (Previously Presented) The method of Claim 7, further comprising a step of collecting the nets having high latency signals into shared interconnect groups.

9. (Previously Presented) The method of Claim 1, wherein the altered netlist comprises a plurality of signal sources in the same configurable logic block.

Claims 10-12. (Cancelled)

13. (Previously Presented) The method of Claim 2, further comprising a step of selecting a source configurable logic block by way of a multi-bit phase bus.

14. (Previously Presented) The method of Claim 13, further comprising a step of allowing a destination configurable logic block to receive signals of any phase of said multi-phase bus.

15. (Previously Presented) The method of Claim 2, further comprising a step of generating a clock signal comprising a global reset signal indicating a first phase to synchronize the plurality of source configurable logic blocks.

16. (Previously Presented) The method of Claim 15, further comprising a step of separately detecting the current time multiplexed phase at each of the source

configurable logic blocks and destination configurable logic blocks.

17. (Previously Presented) The integrated circuit of Claim 3, further comprising a plurality of destinations within the destination configurable logic block, wherein the signal source of the multiple signal sources selected by the time multiplexing signal generator is coupled to one of the destinations within the destination configurable logic block.

18. (Previously Presented) The integrated circuit of Claim 3, further comprising a plurality of destination configurable logic blocks.

19. (Previously Presented) The integrated circuit of Claim 18, wherein the time multiplexing signal generator comprises a multiplexer coupled to the multiple signal sources and controlled by a time multiplexing signal.

20. (Previously Presented) The integrated circuit of Claim 19, wherein each destination configurable logic block comprises a capture device coupled to receive the time multiplexing signal, wherein at least one configurable logic clock is coupled to receive a signal from the selected signal source based upon the time multiplexing signal.